Sequential Symbol Synchronizers based on Clock Sampling by Positive Transitions

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Abstract - **This work presents a sequential symbol synchronizer, that was discovered by us, and its functioning principle is based on the clock sampling by the input positive data transitions.**

This synchronizer has two topologies, namely the discrete and the continuous. Also, each topology has two versions which are the manual and the automatic. These synchronizers are very interesting, because the previous adjust of the manual version isn't critical.

The objective is to study the four synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

This work studies the sequential symbol synchronizer whose functioning principle is based on the clock sampling, by the input positive data transitions.

The input positive data transitions samples the position of the clock negative transition and then the synchronizer corrects this position, becoming it coincident with the positive data transitions [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12].

Only the positive data transitions are used, what can be advantageous in non linear transmission channels.

If this transition clock is delayed then is applied a positive pulse that advances it. However, if the clock is advanced then is applied a negative pulse that delays it.

The clock positive transition samples the data at the symbols center (maximum opening eye diagram).

We will present the two synchronizer topologies (discrete, continuous) each one with two versions (manual, automatic).

Fig.1 shows the blocks diagram of these synchronizers.

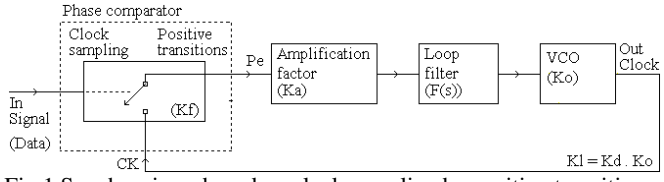

Fig.1 Synchronizers based on clock sampling by positive transitions

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification that controls the root locus and the loop desired characteristics.

Following, we present the discrete synchronizer with its manual and automatic versions.

Next, we present the continuous synchronizer with its manual and automatic versions.

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. DISCRETE SYNCHRONIZER TOPOLOGIES

The discrete topology has a pulse error Pe that advances discreetly until the equilibrium point, without to disappear. This topology has the following manual and automatic versions [1, 2].

A. Discrete topology and manual version

The manual version is based on a delay line that needs a previous human adjustment to produce Pf. This delay isn't critical, but only determines the charge pulse area Pf (Fig.2).

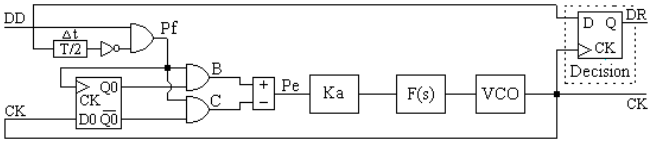

Fig.2 Synchronizer discrete and manual (d-m)

The delay T/2, NOT with 1st AND produces a fixed area pulse Pf that determines the charge rhythm.

Fig.3 shows the waveforms of the synchronizer discrete and manual.

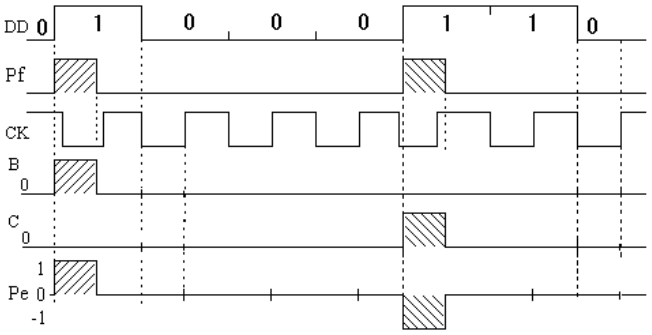

Fig.3 Waveforms of the synchronizer discrete and manual

The error pulse Pe maintains its fixed area during the synchronism process and remains constant at the equilibrium point, only the direction changes.

B. Discrete topology and automatic version

The automatic version is based on a flip flop that automatically provides the delay and variable pulse Pv. This delay determines the charge pulse area Pv (Fig.4).

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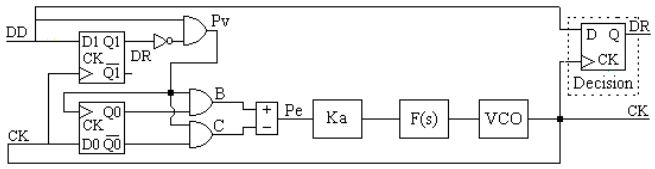

Fig.4 Synchronizer discrete and automatic (d-a)

The flip flop 1, NOT with 1st AND produces a variable pulse Pv that determines the charge rhythm.

Fig.5 shows the waveforms of the synchronizer discrete and automatic.

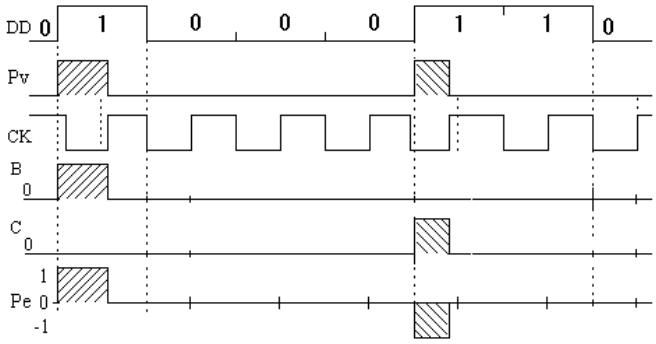

Fig.5 Waveforms of the synchronizer discrete and automatic

The error pulse Pe varies its area during the synchronism, process but remains more or less constant at the equilibrium point.

III. CONTINUOUS SYNCHRONIZER TOPOLOGIES

The continuous topology has a pulse error that advances continuously to the equilibrium point, can change its direction and disappear. This topology has the following manual and automatic versions [3, 4].

A. Continuous topology and manual version

The manual version is based on a delay line that needs a previous human adjustment to produce the fixed pulse Pf.. This delay isn't critical, but only determines the initial charge pulse area A (Fig.6).

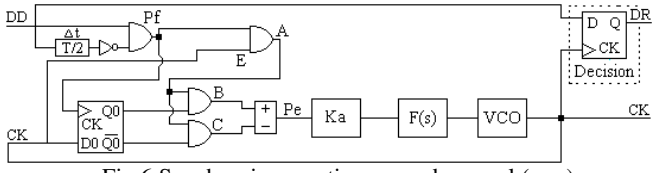

Fig.6 Synchronizer continuous and manual (c-m)

The delay T/2, NOT with the 1st AND produces the fixed pulse Pf and the 2nd AND produces the variable pulse A that determines the charge rhythm.

Fig.7 shows the waveforms of the synchronizer continuous and manual.

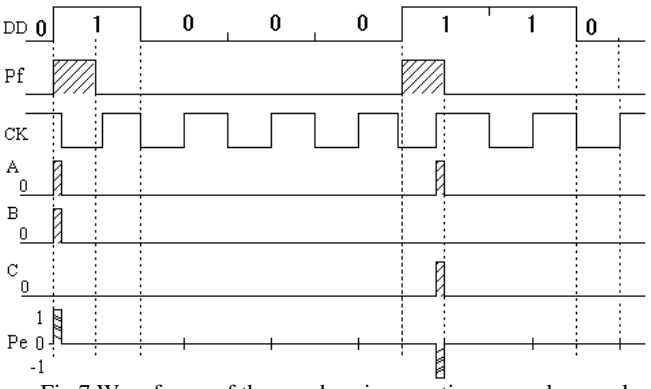

Fig.7 Waveforms of the synchronizer continuous and manual

The error pulse Pe diminishes its area during the synchronism process and disappear at the equilibrium point.

B. Continuous topology and automatic version

The automatic version is based on a flip flop that automatically provides a delay and the variable pulse Pv. This delay determines the initial charge pulse area A (Fig.8).

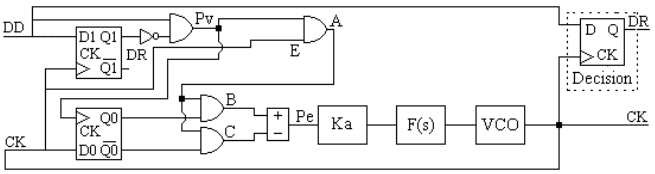

Fig.8 Synchronizer continuous and automatic (c-a)

The flip flop 1, NOT with 1st AND produces a variable pulse Pv and the 2nd AND determines the charge rhythm A.

Fig.9 shows the waveforms of the synchronizer continuous and automatic.

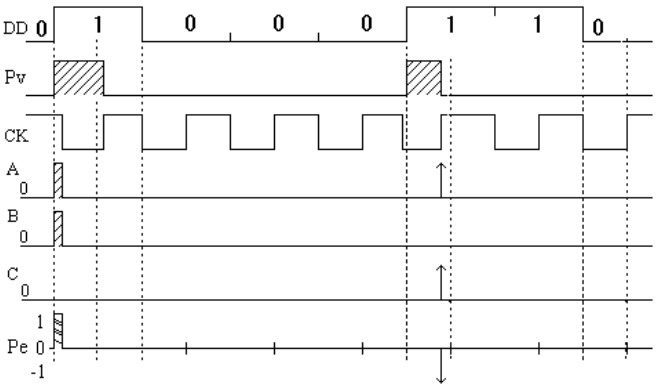

Fig.9 Waveforms of the synchronizer continuous and automatic

The error pulse Pe diminishes its area during the synchronism process and disappear at the equilibrium point.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = A^2_{ef}/(No.Bn). But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then No=2σn^2.Δτ, so SNR=A^2_{ef}/(2σn^2.Δτ.Bn) = 0.5^2/(2σn^2*10^{-3}*5)= 25/σn^2.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is
Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=1/2; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2/π* (3)

For the hybrid synchronizers, the loop bandwidth is
Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=0.45; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2.2/π* (4)

For the combinational synchronizers, the loop bandwidth is
Bl=0.02=(Ka.Kf.Ko)/4 with (Kf=1/π; Ko=2π)

*(Ka*1/π*2π)/4 = 0.02 -> Ka=0.04* (5)

For the sequential synchronizers, the loop bandwidth is
Bl=0.02=(Ka.Kf.Ko)/4 with (Kf=1/2π; Ko=2π)

*(Ka*1/2π*2π)/4 =0.02 -> Ka=0.08* (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.
For analog PLL the jitter is
$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$
For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

Following Fig.10 shows the setup that was used to test the various synchronizers.

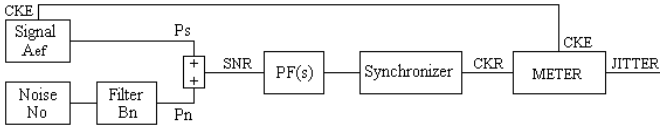

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

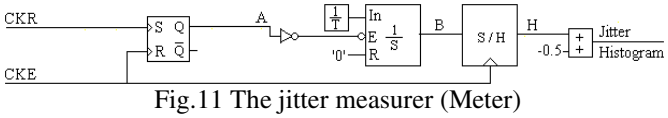

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.
Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter UIRMS versus input SNR) for the four synchronizers.

Fig.12 shows the jitter-SNR curves of the four synchronizers namely the discrete and manual (d-m), the discrete and automatic (d-a), the continuous and manual (c-m) and the continuous and automatic (c-a).

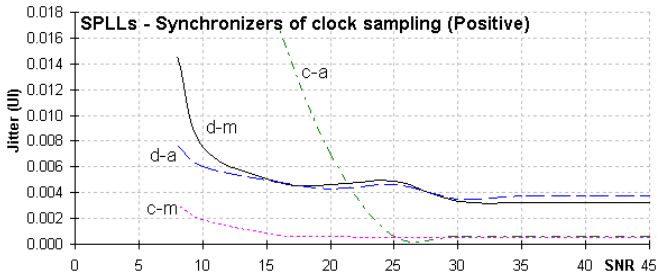

Fig.12 Jitter-SNR curves of the four synchronizers(d-m,d-a,c-m,c-a)

We see, that generally the output jitter UIRMS diminishes gradually with the input SNR increasing.

For high SNR, the four curves tend to be equals, but with some advantage of the continuous topologies (c-m, c-a). However, for low SNR, the continuous manual (c-m) is the best, followed similarly of the discrete topologies (d-m, d-a) and the continuous automatic (c-a) is the worst.

V. CONCLUSIONS

We studied four synchronizers, namely the discrete manual (d-m), the discrete automatic (d-a), the continuous manual (c-m) and the continuous automatic (c-a). Then, we tested their output jitter UIRMS versus input SNR.

We observed that, generally, the jitter UIRMS diminishes gradually with the SNR increasing.

We verified, that for high SNR, the jitter of the four synchronizers is similar, but with a slight advantage of the continuous topologies (c-m, c-a). This is comprehensible since the error pulse Pe, in discrete topologies, don't disappear at the equilibrium point, only changes its direction.

However, for low SNR, the continuous manual (c-m) is the best, this is comprehensible since the error pulse Pe diminishes gradually and disappear at the equilibrium point, also the additional AND is a closed door to the noise. The discrete topologies (d-m, d-a) have an intermedium performance since their error pulse Pe don't disappear at the equilibrium point. The continuous automatic (c-a) has the worst jitter, since its error pulse Pe has a non symmetric positive and negative pulse contributions, what degrades the jitter.

ACKNOWLEDGMENTS

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